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# OBPSR: A Multi-signal Receiver Based on the Orthogonal and Bandpass Sampling Techniques

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**Abstract**—Multi-signal receivers with integrated functions in the receive/transmit chain are desired in Wireless technology devices such as Smartphones, due to processing time, cost and size saving. This paper proposes a new multi-signal receiver design that formats signals orthogonally for processing by a single Costas Quadrature Phase-Locked-Loop CQPLL; thus allowing the digital processor to switch from tracking/decoding any one of the received signals to the other without losing phase lock or time. Our receiver utilizes a Hilbert Transform for shifting one of the signals by  $90^\circ$  to prevent overlapping before using Bandpass sampling to fold the two signals to the same frequency in the First Nyquist Zone. The resultant orthogonal kernels are fed to a single CQPLL for tracking and demodulation. Matlab simulations prove our new technique that also reduces the sampling frequency to a rate proportional to the maximum bandwidth, instead of the summation of bandwidths, of the input signals.

**Keywords**—component; Orthogonal signals, BPSR, multi-signal receiver, PLL, signal tracking

## I. INTRODUCTION

Production of multi-frequency RF transceivers used in Smartphones and other wireless devices is expected to reach 1.5 billion in 2015 [1]. A typical Smartphone will include many wireless technologies such as Wi-Fi, Bluetooth and GNSS. Therefore sharing parts of the received signal chain functions will help reduce hardware cost, size, processing time and power consumption.

The integration of wireless transceivers is a major research area under the umbrella of software defined radio (SDR) and cognitive radio [2]. The BandPass Sampling technique (BPS) has been the focus of many solutions based on folding the entire signal input spectrum to specific zones [3].

This paper proposes to reformat the input signals to be orthogonal to each other before a BPS receiver stage to allow a single Phase Lock Loop (PLL) be used to track all received signals at once. For a two signal receiver; our solution employs a Hilbert Transform (HT) for shifting one of the input signals by  $90^\circ$  [4]. Then, using the BPS technique, we fold back the two received signals to the same reference frequency in the First Nyquist Zone (FNZ). Note that, the folded

information bandwidth of the two signals over each other will not cause interference between the information of the folded signals because they are orthogonal (due to using HT that has made  $90^\circ$  deference between the information). This will produce an orthogonal signal, which is passed to a single CQPLL for tracking and demodulation as shown in Fig 1. The CQPLL is chosen over the QPLL because it does not have an extra loop present in QPLL used to assure accuracy of the in-phase and quadrature amplitudes that are not necessary here and thus saving processing time and implementation.

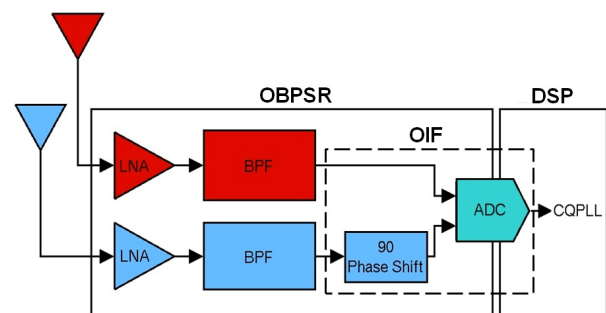


Figure 1. Orthogonal BandPass Sampling Receiver (OBPSR)

Our proposed Orthogonal BandPass Sampling Receiver (OBPSR) is designed to capture two signals simultaneously and use a single channel in the digital domain for processing them, including tracking and decoding, concurrently. This is equivalent to a saving of a complete single receiver chain. In addition, we chose the minimum sampling frequency based on the “maximum of the input signals bandwidth” rather than the “summation of the input signals bandwidth”; thus reducing the number of samples and saving processing time.

The rest of this paper is organized as follows: Section II surveys the literature for published BPS and PLL techniques for multi-signal solutions. In the section III, we describe this proposed receiver (OBPSR) in detail with the mathematical prove. Section IV describes the simulation of the experimental set-up that has been used to evaluate OBPSR, while section V discusses the experimental results. Section IV concludes this work together with future work plans.

## II. BACKGROUND

### A. The Bandpass sampling technique

Bandpass sampling refers to an established front-end technique where analogue multi-bandpass signals are down-converted (or folded) to baseband in the FNZ. This is achieved by placing the Analogue-to-Digital Converter (ADC) as near to the antenna as possible; without utilising an analogue mixer, local oscillator and image filters.

For a multi-signal receiver, a suitable sampling frequency is chosen so to prevent overlapping between all the folded kernels of these received signals in the FNZ [5]. As a minimum, this sampling frequency has to be double the bandwidth of the combined received signals bandwidths. Therefore, the sampling frequency becomes a tiny proportion of the carrier frequency of the received signals; thus reducing the samples processing and in turn reducing the power consumption while handling multi-signals at the same time (especially when measured in comparison with traditional receivers). This saving is very important to the implementation of multi-signal receivers readily used in Smartphones.

Equation (1) shows the mathematical relationship defining the folding frequency of a single received signal in the FNZ based on its carrier frequency and the chosen sampling frequency.

$$f_{\text{fold}} = \begin{cases} \text{rem}(f_c, f_s) & \text{if } \text{fix}\left(\frac{f_c}{0.5 * f_s}\right) \text{ is even} \\ f_s - \text{rem}(f_c, f_s) & \text{if } \text{fix}\left(\frac{f_c}{0.5 * f_s}\right) \text{ is odd} \end{cases} \quad (1)$$

Where  $f_{\text{fold}}$  is the folded frequency,  $f_s$  is the sampling frequency,  $f_c$  is the carrier frequency,  $\text{fix}(f_c/0.5*f_s)$  is the truncated portion of  $f_c/0.5*f_s$  and  $\text{rem}(f_c, f_s)$  is the remainder of  $f_c/f_s$ .

One of the objectives of our multi-signal receiver is to not only to save in the processing of front-end, but also to be able to switch the digital processing of any one of the received signals to another and vice-versa without losing lock with any of the received signals. To enable us to use the CQPLL, this meant that our proposed 2-signal receiver has to have a suitable sampling frequency that will fold both of our received signals to the "same" frequency in the FNZ as well as conforming to equation (1). An iterative process was therefore programmed to calculate this required sampling frequency based on the exact type of received signals.

The first generation of the multi-signal down-conversion receivers which has the following limitations; 1) requiring wideband ADC which is impractical, 2) requiring a high quality (expensive) analogue BandPass Filter (BPF) after the antenna to remove all noise from the received signals so to avoid the noise being folded back with the signal, 3) ideal for use with single side band signal (or upper side of double side-lobe signal) transmission so to avoid overlapping and crowding the spectrum of the folded signals in the FNZ caused by the lower-side part of the signal [5].

To ensure that only a single-side lobe of any double-lobe signals are processed by the BPS technique, an HT can be used

to cut-off the lower-side lobe of such signals. This is achieved by splitting the received signals into two paths. The Q-component path passes through an HT filter before an ADC, while the I-component path of the signal is passed to an ADC directly and then recombined with shifted signal from the Q-component path [6]. This technique will eliminate the negative frequency part of the input signals spectrum.

To avoid the need for using a wide ADC as well as a high quality filter in BPSRs, designers were converting the frequencies of the received signals to be at the zero frequency in the FNZ. This is done based on multiplying the received signals (after the signals have been passed through a bank of bandpass filters and low noise amplifiers) with a down-conversion function that converts the received signals directly to baseband signals at zero frequency. This down-conversion function will also produce inter-modulation and second harmonics components. A minimum frequency separation technique is used to force the locations of the inter-modulation components in the baseband to be greater than certain minimum value! This is so that an anti-aliasing filter can be deployed to allow the baseband signals only that are then passed into an ADC [7]. This will greatly simplify the design of the ADC as it only needs to handle baseband signals. However, such down-conversion function has a drawback in that it also generates undesired nonlinearity and ISI that will add distortion to the in-band signals. Furthermore, converting the frequencies to the zero frequency in the FNZ introduces a DC offset that will cause an I-Q mismatch.

To overcome this DC offset problem, our proposal is to fold the received signals to any non-zero frequency in the FNZ. In addition, our OBPSR's Integrated Function (OIF) produces an orthogonal signal and so eliminates the ISI problem. Furthermore, in our BPS receiver, the tracking and demodulation (I-Q match) of the acquired signals will be a digital task and so obtaining adequate matching accuracy in the digital signals can be easily accomplished.

### B. The Phase locked loop

The PLL is an essential function used for coherent carrier tracking of the received signal based on comparing the phase values of the received signal with a locally generated signal. i.e., the principle idea of the PLL is to generate a known reference signal that locks to the phase (tracking) of the received signal.

The conventional PLL consists of three main functional units; 1) Phase Detector (PD), 2) Loop Filter (LF), and 3) Voltage-Controlled Oscillator (VCO). The PD starts to compute the phase error, when the PLL has been locked to the received signal phase. This phase error is then filtered through the LF and is used to drive the VCO to generate the reference signal, which now instantaneously follows the received signal phase [8]. Besides the phase error, the PD mechanism of the conventional PLL naturally produces unwanted double-frequency ripples that will directly impact on the estimation of the received signal's phase.

The Enhanced-PLL (EPLL) overcomes the shortcoming of the conventional PLL by adding a new magnitude-estimator loop to the PD that will optimise the received signal to a well-

defined-error-signal using a gradient-descent method (GDM), where the received signal will not be multiplied directly with the output of the VCO; instead, it will go through a pre-processor before being multiplied [9]. i.e., the output signal of the magnitude-estimator loop is subtracted from the received signal to produce a well-defined-error-signal. This error signal is then passed through two branches in the PD: 1) the error signal is multiplied by the in-phase component of the reference signal and then passed to a traditional PLL to estimate the phase and the frequency. 2) the error signal is multiplied by the quadrature component of the reference signal and then passed to the magnitude-estimator loop to determine the amplitude and the phase-angle. This estimation uses GDM to achieve precise convergence with the received signal, thus eliminating the impact of double-frequency ripples. However, the GDM requires significant computational time to obtain a good estimation, thus limiting the use of EPLL in some applications such as Smartphones. The Newton's method [10] and the Relaxation Iteration method [11] were proposed to reduce this GDM computational time.

The QPLL is designed to track Quadrature Phase Shift Keying (QPSK) signals. The QPLL is an extended version of the EPLL, incorporating new parameters in the PD that will control estimating the in-phase amplitude, the quadrature amplitude and phase components of the received signal. The PD of the QPLL consists of two, in-phase and quadrature-phase, branches, each of which contains three Multipliers, two gain Amplifiers, an Integrator and an Adder. Another Adder is then used to sum-up the signals coming from these two branches. This combined signal is then subtracted from the actual received signal to produce the error signal. This error signal is then used to adaptively estimate the amplitudes components and the phase [12].

The QPLL is an improved version of the CQPLL. The PD mechanism of the QPLL is more sophisticated than the PD of the CQPLL and so requires more computational time. The CQPLL is specifically designed to track and decode unbalanced QPSK signals [13]. Therefore, the CQPLL makes the best candidate for our proposal since the received orthogonal signals will have different average power. Also, we chose the CQPLL to save computational time during tracking and decoding.

As shown in the Fig. 2, the PD of the CQPLL consists of four Multipliers, two LPFs, two Hard-limiter functions and one Adder. Again, the received signal is processed through two branches; the output signal of the in-phase branch is multiplied with output of the hard-limiter function of the quadrature component. The resultant is then subtracted from the multiplication of the quadrature component of the baseband signal with output of the hard-limiter function of the in-phase component. This subtraction produces an error signal. This error signal is amplified and filtered by a Loop Gain (LG) and LF respectively, and then it is used to adjust the phase of the reference signal (VCO) with respect to the previously processed received signal. The output is then fed back to the PD block by the quadrature reference signal (I-arm & Q-arm) to close the loop.

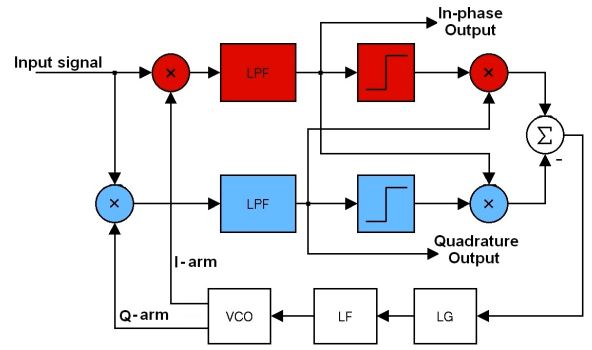


Figure 2. Costas Quadrature Phase Locked Loop (CQPLL)

### III. OBPSR ARCHITECTURE

As shown in Fig. 1, our proposed 2-signals OBPSR architecture consists of two Low-Noise Amplifiers (LNA), two BPFs, a 90° phase-shifter and an ADC. The phase shifter (Hilbert Transform) and the ADC make up the OIF used for harmonizing the orthogonality of the filtered received signals. As shown in Fig. 3, the HT is used as the first stage for shifting the phase of the second received signal by 90° to prevent the signals overlapping prior to using the BPS technique. By choosing an appropriate sampling frequency, the second stage uses a BPS technique to fold both received signals (now orthogonal) to the same fold-frequency in the FNZ. Thus producing an orthogonal baseband signal that is fed into a single CQPLL to track and decode the signal. This makes both signals' information available at the same time and effectively reducing the tracking channels in the digital domain to half.

Our OBPSR also reduces the sampling rate such that it is proportional to the maximum bandwidth of the received signals instead of the summation of the two signals bandwidths. This will significantly reduce the processing time in the digital domain. In addition, the OBPSR can be used cluster the spectrum of the received signals based on choosing the sampling frequency that folds each two signals to one specific band in the NZ's.

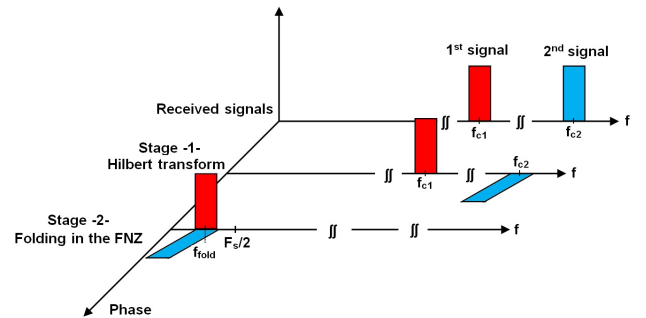


Figure 3. Frequency and phase representation of the OBPSR integrated function

Equations (2) and (3) represent two Binary Phase Shift Keying (BPSK) bandpass signals  $S_1$  and  $S_2$  that are received through Additive White Gaussian Noise channel (AWGN).

$$S_1 = A_1 \cos(2\pi f_{c1} t + m_1) + n_1 \quad (2)$$

$$S_2 = A_2 \cos(2\pi f_{c2} t + m_2) + n_2 \quad (3)$$

Where,  $(A_1, f_{c1}, n_1)$  and  $(A_2, f_{c2}, n_2)$  represent the amplitude, the carrier frequency and the Gaussian noise of the first and second signals respectively.  $m_1$  and  $m_2$  represent the information message of the first and second signals respectively, and can be expressed as:

$$m_1 = \pi(1 - b_1), \text{ where } b_1 = 0,1 \text{ bits}$$

$$m_2 = \pi(1 - b_2), \text{ where } b_2 = 0,1 \text{ bits}$$

As described earlier, by applying HT to (3), then summing with (2) we will generate the signal that will be folded to the FNZ as shown in (4)

$$S_{\text{dig}} = \pm A_1 \cos(2\pi f_{\text{fold}}t) \pm A_2 \sin(2\pi f_{\text{fold}}t) + N \quad (4)$$

Where,  $S_{\text{dig}}$  is the orthogonal digital signal at the fold frequency ( $f_{\text{fold}}$ ) and it carries two different information messages  $m_1$  and  $m_2$ .  $N$  represents the combined noise  $n_1+n_2$ .

#### IV. EXPERIMENTAL SET-UP

MATLAB is used to simulate our OBPSR proposed technique. To represent the transmitted signals, two BPSK modulated signals with 1 MHz bandwidths (1 Msymbols/s) are passed through a "root raised cosine filter" with a roll-off factor of 0.2. Two different carrier frequencies of 1575 MHz and 1605 MHz are used for the first signal and the second signal respectively. AWGN is then used to simulate transmission channel noise. Simulation is run for 10 mseconds which represents 10000 bits of data.

These two simulated signals once captured by their respective antennas, are passed through LNAs and two narrow BPF's centred on carrier frequencies of 1575 MHz and 1605 MHz to eliminate all frequencies outside the signals bandwidth. The resulted in-band signals are then fed to the OIF. Note that the phase of the 1605 MHz signal is shifted 90-degree and combined with the 1575 MHz signal in order to digitize them, at the same time, by a 10-bit ADC, with 12 MHz sampling frequency. A 12 MHz sampling frequency is chosen so the ADC folds the combined signal and its images to the desired zone; in our case, we selected FNZ as shown in Fig. 4. The output orthogonal digital signal is then processed through a CQPLL for tracking and extracting the information data/messages. Note that the CQPLL function is implemented in MATLAB too.

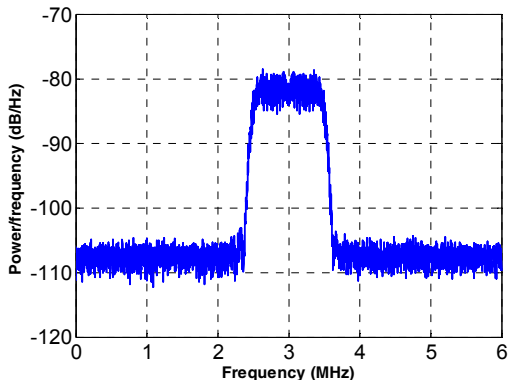


Figure 4. Power spectral density of the orthogonal signal in the FNZ

#### V. EXPERIMENTAL RESULT

Adjacent Channel Power Ratio (ACPR), Bit Error Rate (BER) and Error Vector Magnitude (EVM) are used to: (a) Analyse the effect of the OIF on the in-band/out-of-band of the desired signal spectrum in terms of the re-growth in bandwidth, the total power and the adjacent channels effect. (b) Checking the behaviour of the CQPLL during tracking the orthogonal signals, and (c) Evaluate the overall performance of the OBPSR.

The following discussion documents our findings:

1. Readings of high and low ACPR measurements of the signals after and before the OIF are shown in table I.

TABLE I. SIMULATED POWER MEASUREMENT FOR INPUT AND OUTPUT SIGNALS OF PROPOSED ARCHITECTURE

	Main channel power	ACPR Low	ACPR High
Signal before the OIF (the first signal)	5.24 dBm	-34.61	-34.59
Signal before the OIF (the second signal)	5.20 dBm	-34.64	-34.61
Signal after the OIF (the orthogonal signal)	8.26 dBm	-34.56	-34.57

This shows a slight increase of about 3 dB in the main channel power, which proves that the spectrum of the OIF output signal (the orthogonal signal) has no re-growth. Note that these ACPR values are high but we have concluded that these are acceptable for our example simulation because ACPR values are dependent on the type of signal evaluated [14]. For example the acceptable value for WCDMA signals is -45 dBc for high and low ACPR @ 5 MHz offset, while acceptable value is -33 dBc for QPSK subcarrier modulation signal. Also, note that the value of the main channel power has increased by 3dBm after applying the OIF which means that the noise has also increased by the same value. This extra noise has an insignificant effect on the OBPSR performance, as discussed in (3).

2. As shown in Fig. 5, The CQPLL has a steady-state value during tracking the two signals.

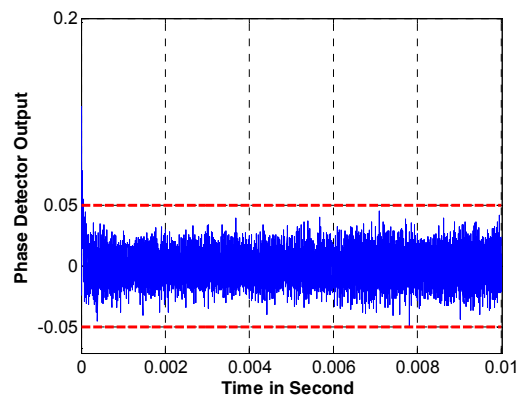


Figure 5. The steady-state of the CQPLL discriminator



This proves a successful process in the OIF to achieve the orthogonality between these signals. Otherwise, we will notice a significant fluctuation in the phase difference (unsteady-state) of the CQPLL due to the presence of offset frequency between the folded frequencies of these signals in the FNZ. However, this stability in CQPLL does not mean that the estimated in-phase and quadrature-phase are identical to the actual value of the in-phase and quadrature-phase of the received signals.

3. The 3 dB extra noise gathered with our orthogonal signal is due to the OIF. The BER versus the energy per bit to noise power spectral density ratio ( $E_b/N_0$ ) is therefore measured, as shown in Fig. 6, which illustrates a small increase in the value of the BER of the OBPSR in comparison with the theoretical value. Besides, the curve of the BER of the OBPSR is approximately identical to the curve of the BPSR. Note that the BPSR setup is same as the OBPSR (one input signal (BPSK)). Consequently, the extra noise has insignificant effect in the performance of our receiver.

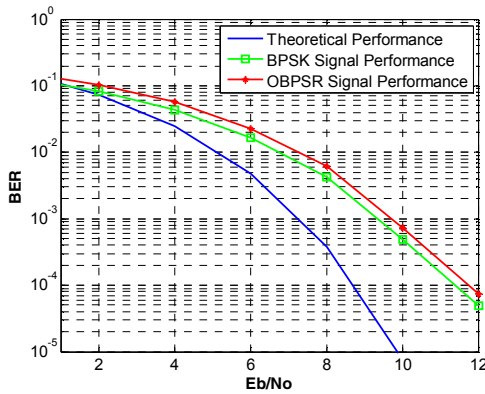


Figure 6. Bit error rate curves for BPSK, QPSK, and orthogonal signal, AWGN channel.

4. The EVM is used to help us define the difference between the estimated complex voltage of the demodulated symbol and the value of the actual received symbol. The new phase of the orthogonal signal we generate has been shifted up and down from its original position. EVM can precisely examine the shifting operation of our OIF we well as help us evaluate the effect of ISI. In order to measure EVM correctly, we have generated a reference signal based on (4), but without the noise component and this will be compared with the estimated signal using the BPSR setup. Table II shows the values of the  $EVM_{RMS}$  and the maximum EVM peak of the OBPSR.

TABLE II. EVM VALUES FOR BPSK AND ORTHOGONAL SIGNALS

	$EVM_{RMS}$	EVM max peak at symbol
OBPSR	6.02 %	16.53 %
BPSR	5.85 %	16.66 %

The estimated phase and amplitude of the orthogonal signal are approximately matching to the value of the reference signal. Also, the performance of the OBPSR is almost identical to that of the BPSR, indicating that there are no ISI in our receiver, also shown in Fig 7. This further proves

that the shifting operation during the OIF has been carried out accurately.

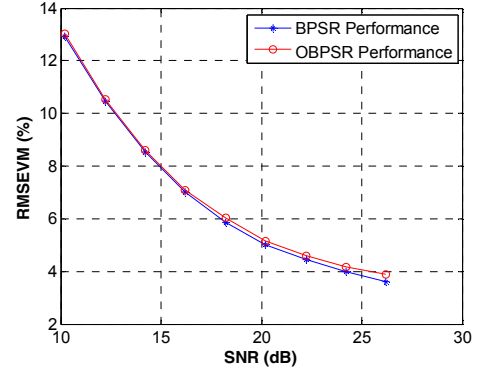


Figure 7. Error vector magnitude curve (RMS) for BPSK and the orthogonal signals

## VI. CONCLUSIONS

This paper proposes a new multi-signal receiver (OBPSR) that has the ability to capture and track multiple signals simultaneously (our implemented scenario was for 2-signals receiver). The novelty of this work is centred on the OIF that continuously harmonies the two received signals to form a single orthogonal signal allowing the “tracking and decoding” to be carried out by in single CQPLL in the digital domain. Thus save in valuable attributes such as device and manufacturing costs, circuitry power dissipation and processing time when compared with conventional side-by-side receivers.

Our simulation result of various types of signals and scenarios proves that the OBPSR design is accurate in integrating the received signals thus producing one-to-one estimation of recovered message data.

This work is part of an on-going DPhil research that includes handling more than two signals in the receive chain aimed at Smartphone transceivers.

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